

	L #	Hit	Sear h T xt	DBs
1	L1	2317	(174/255,260).ccls.	USP AT; US-P GPU B
2	L2	1111	(361/792,793,794,795).c cls.	USP AT; US-P GPU B
3	L3	3126	1 2	USP AT; US-P GPU B
4	L4	1066	3 and (ground (power voltage reference) adj (layer\$1 plane\$1))	USP AT; US-P GPU B
5	L5	366	4 and (capacitor\$1 condenser\$1)	USP AT; US-P GPU B
6	L6	20	4 and (parasitic with (capacitor\$1 condenser\$1))	USP AT; US-P GPU B
7	L7	513	361/803.ccls.	USP AT; US-P GPU B

	L #	Hit	S arch T xt	DB
8	L8	171	7 and (ground (power voltage reference) adj (layer\$1 plane\$1))	USP AT; US-P GPU B
9	L9	60	8 and (capacitor\$1 condenser\$1)	USP AT; US-P GPU B
10	L10	414	5 9	USP AT; US-P GPU B
11	L11	3	8 and (parasitic with (capacitor\$1 condenser\$1))	USP AT; US-P GPU B